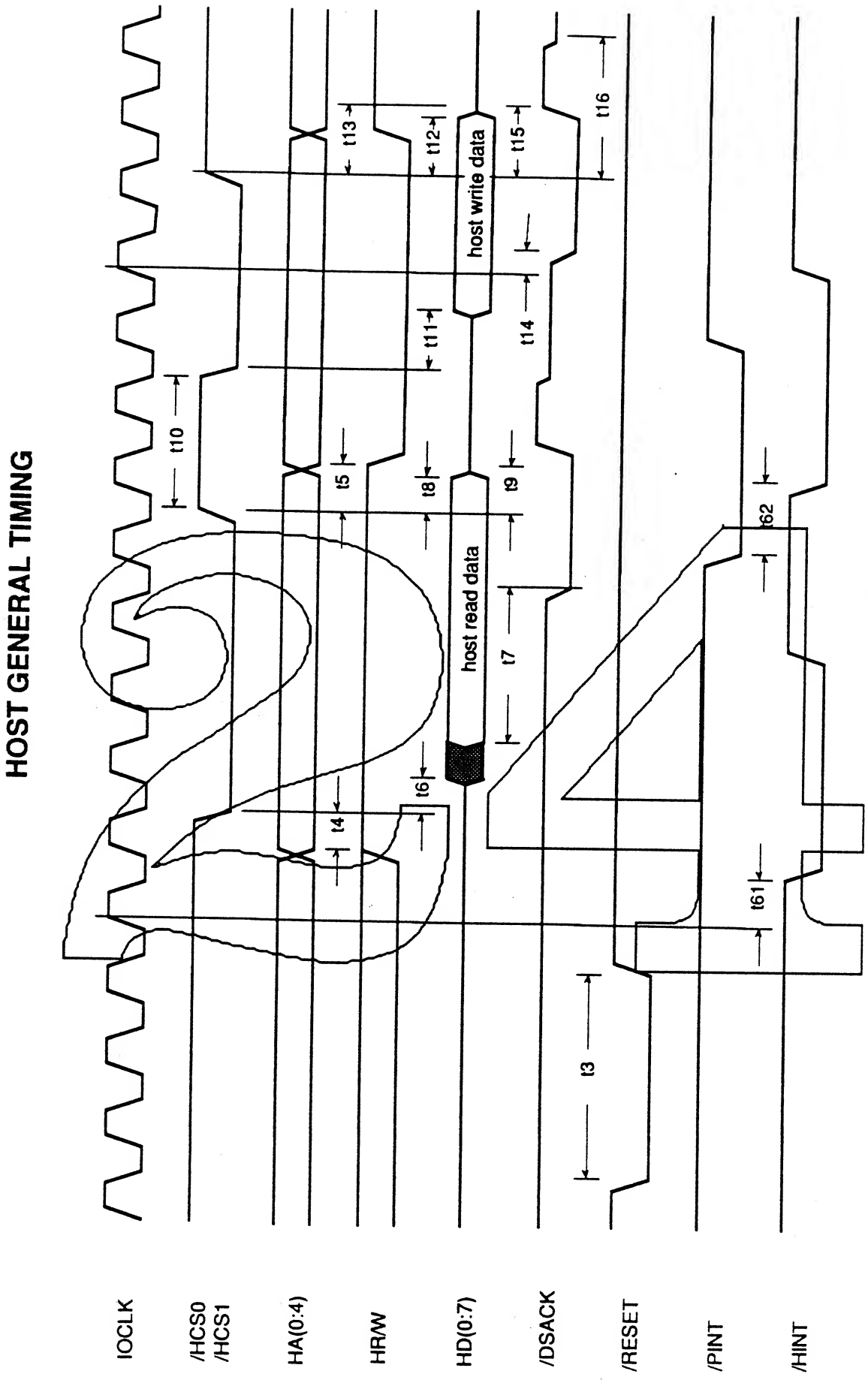

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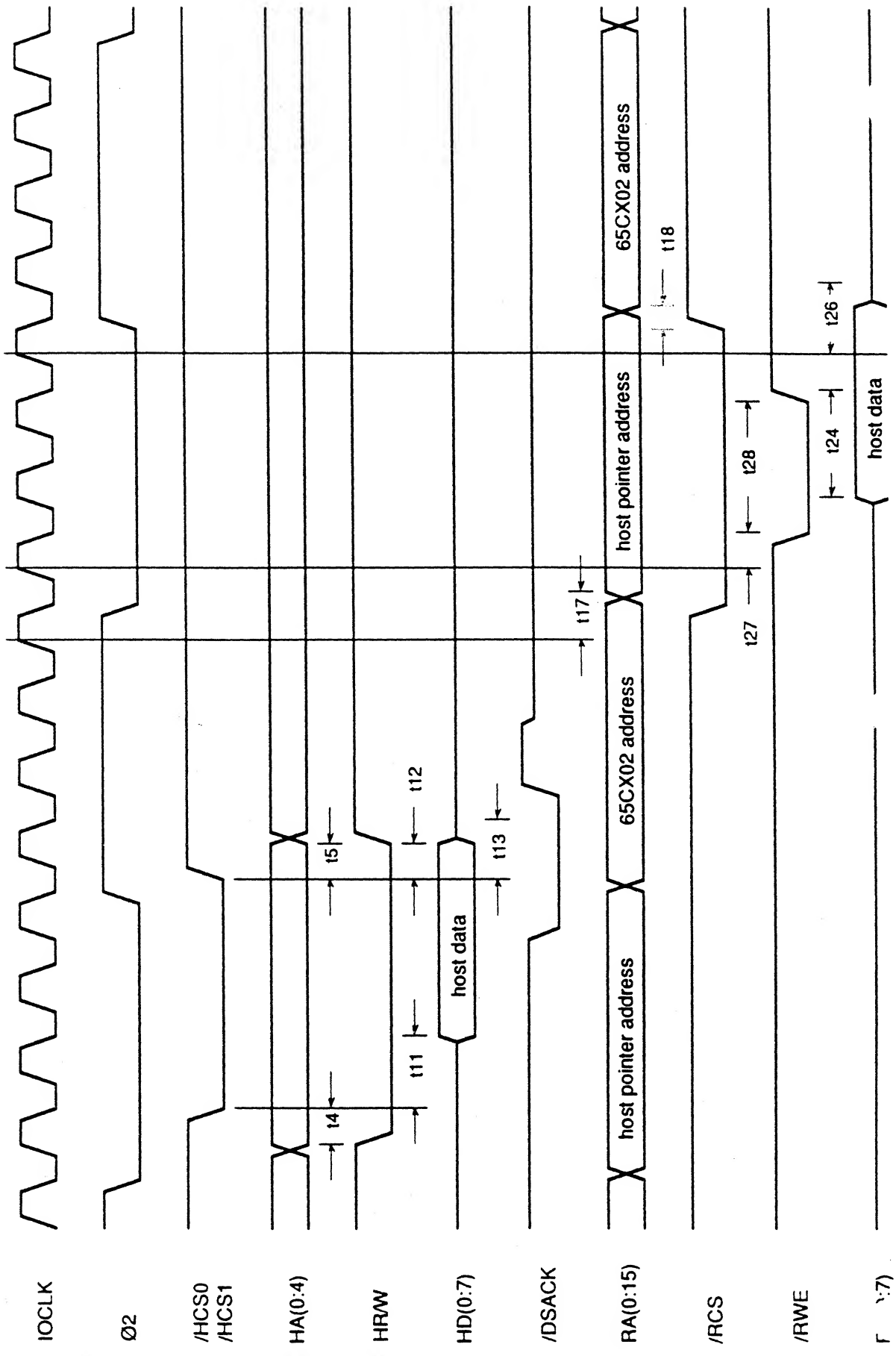
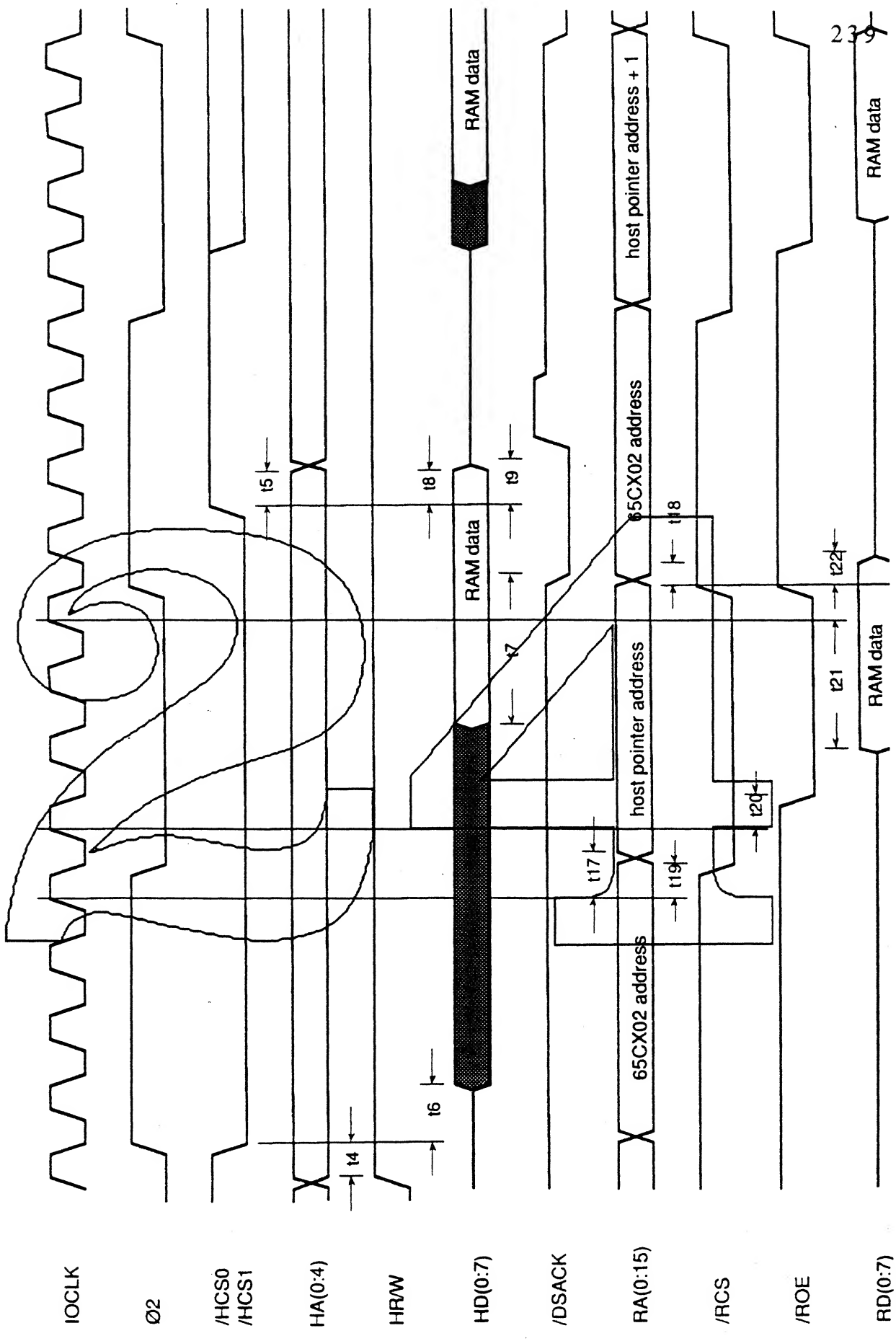
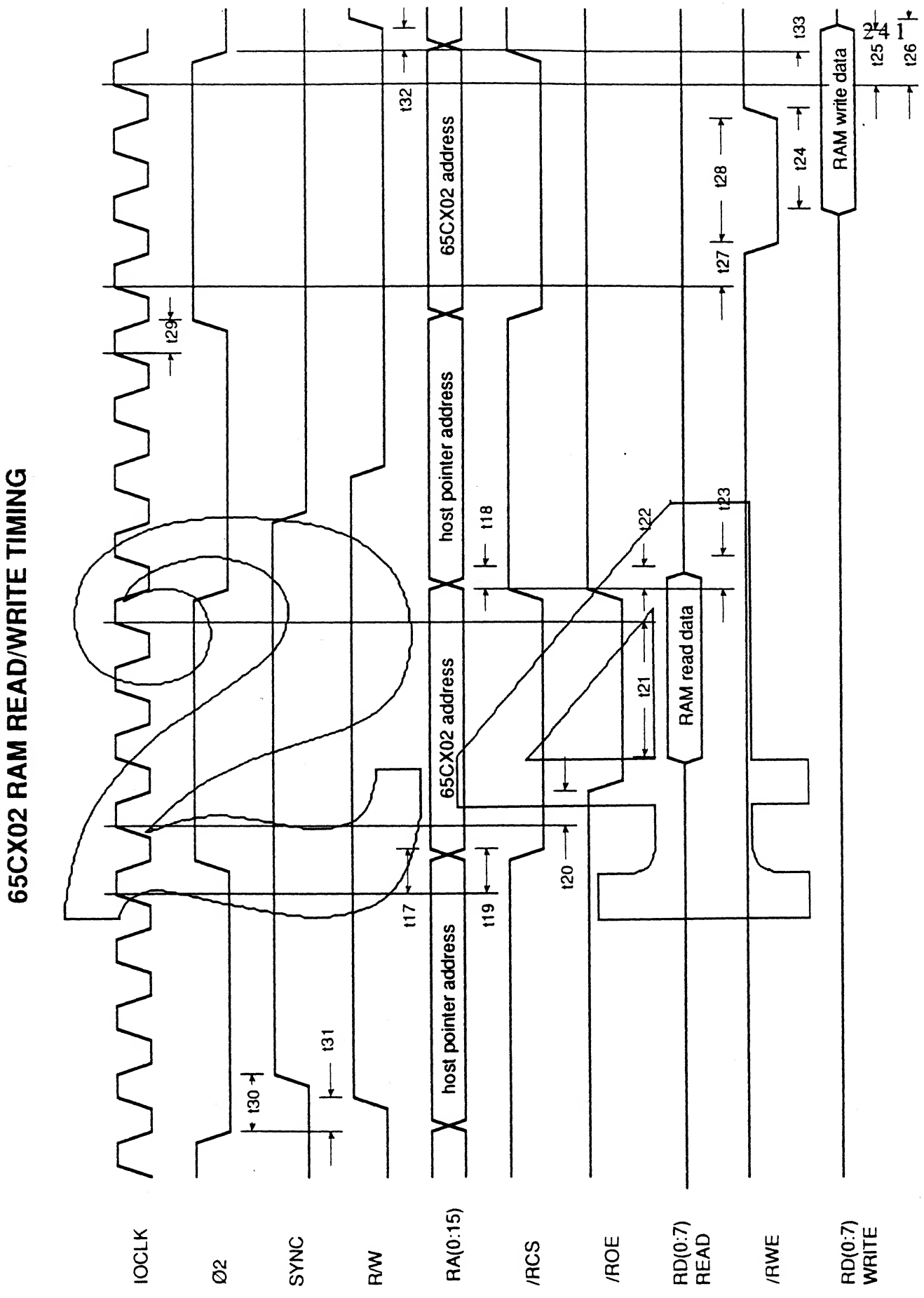
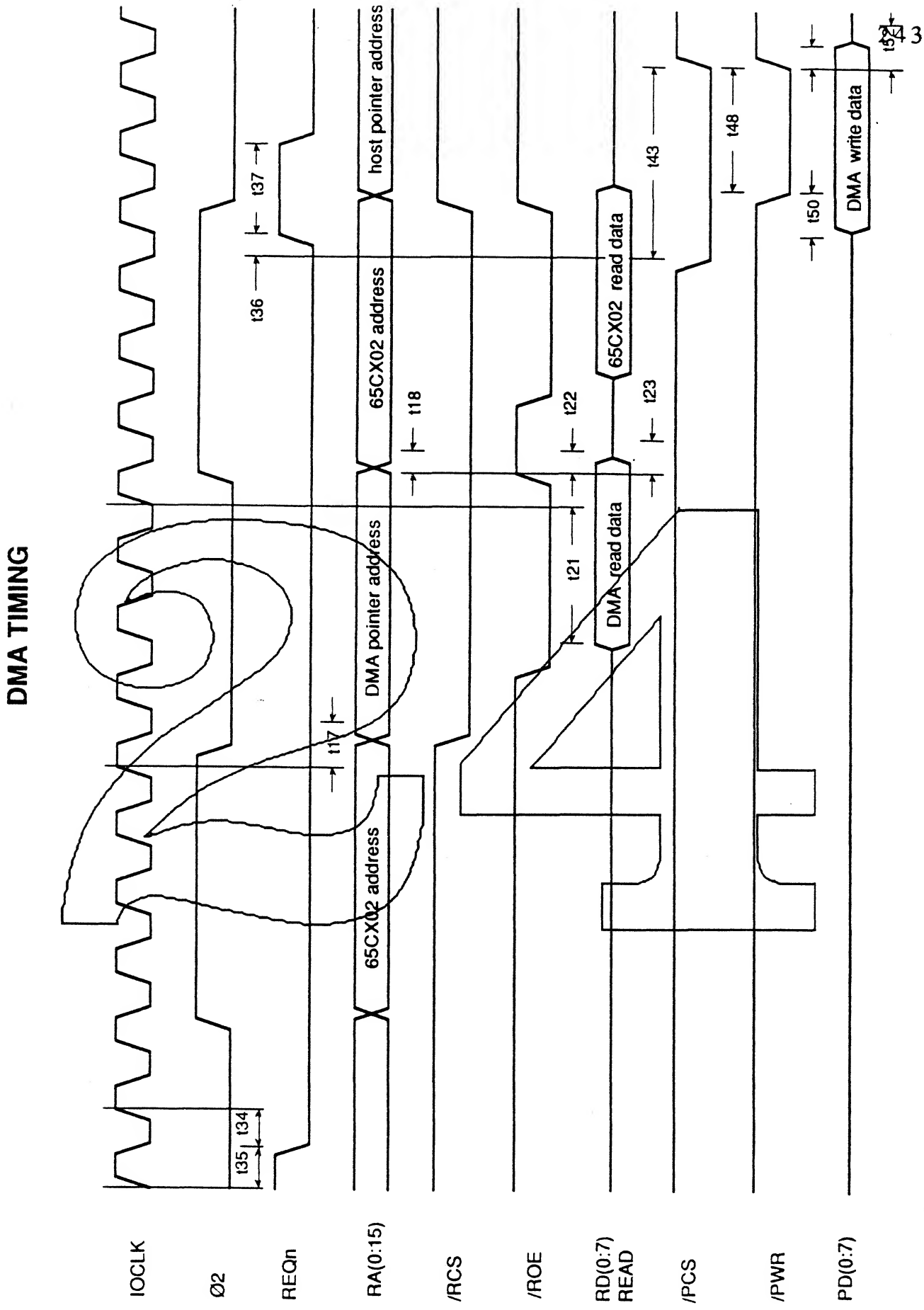
HOST RAM WRITE TIMING

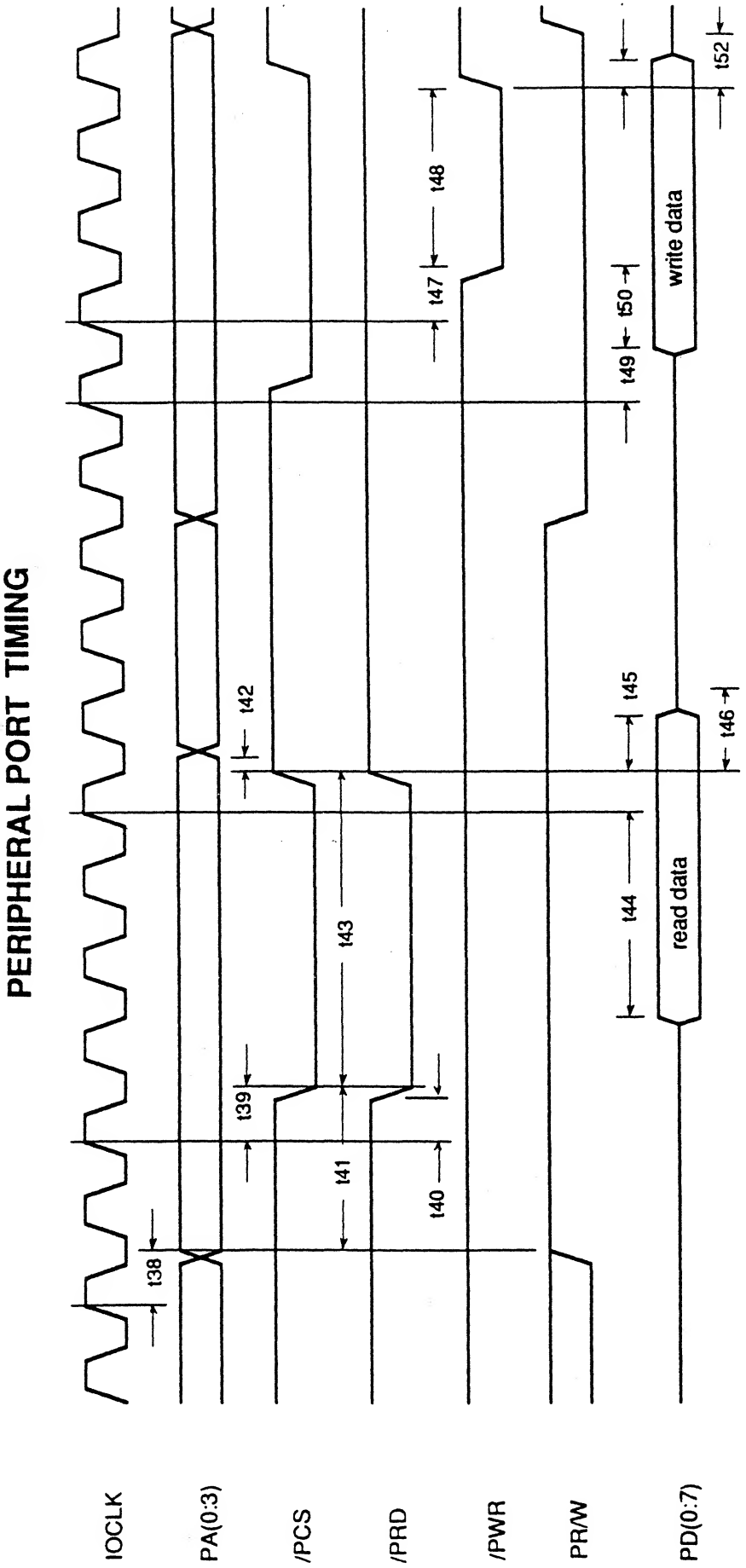


HOST RAM READ TIMING




65CX02 RAM READ/WRITE TIMING
IOCLK
Ø2
SYNC
R/W
RA(0:15)
/RCS
/ROE
RD(0:7) READ
/RWE
RD(0:7) WRITE
host pointer address
65CX02 address
host pointer address
65CX02 address
RAM read data
RAM write data
t17
t18
t19
t20
t21
t22
t23
t24
t25
t26
t27
t28
t29
t30
t31
t32
t33


DMA TIMING
IOCLK
Ø2
REQn
RA(0:15)
/RCS
/ROE
RD(0:7)
READ
/PCS
/PWR
PD(0:7)
t34
t35
t36
t37
t117
t118
t21
t22
t23
t43
t48
t50
t52
65CX02 address
DMA pointer address
host pointer address
65CX02 address
DMA read data
65CX02 read data
DMA write data



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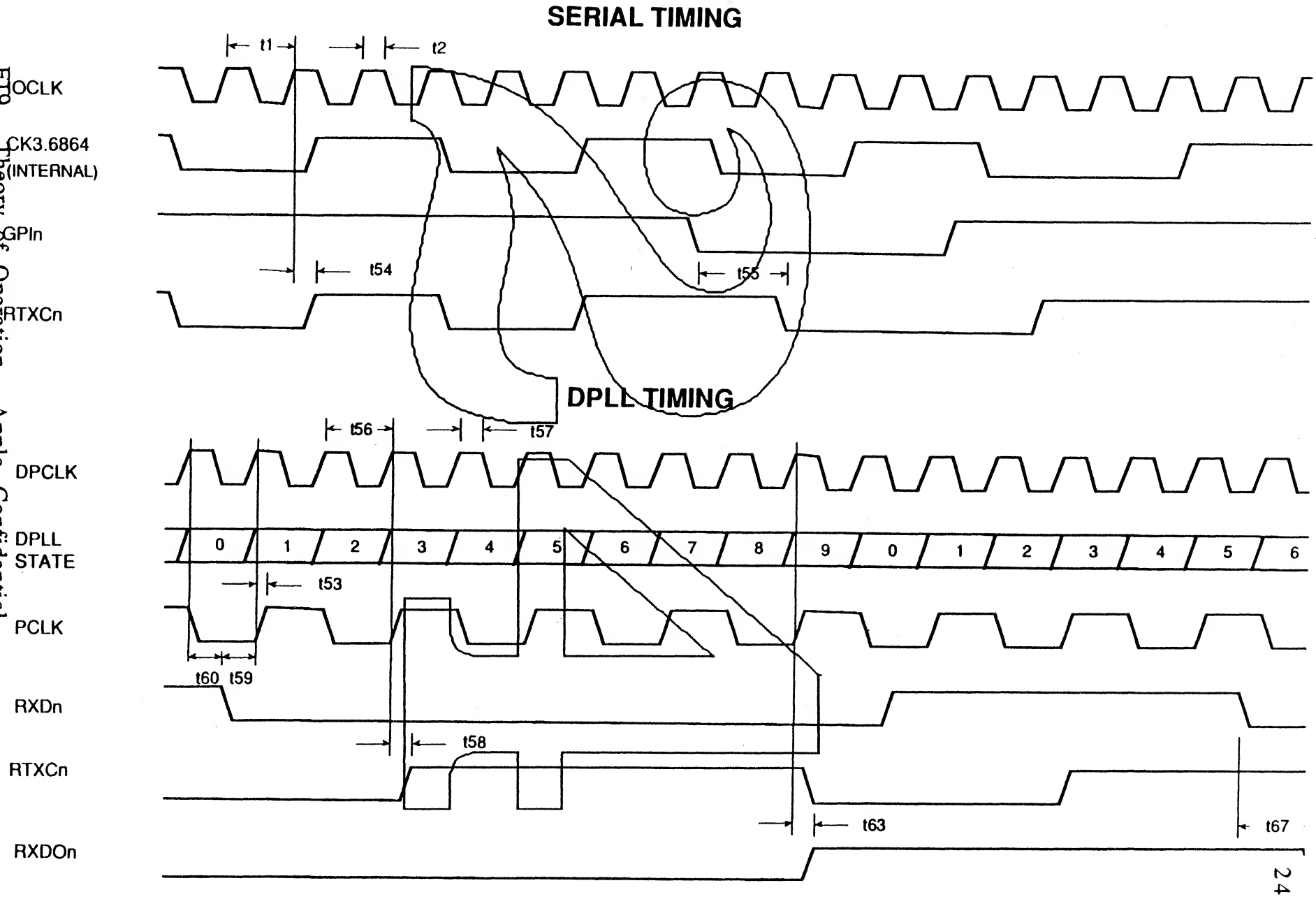
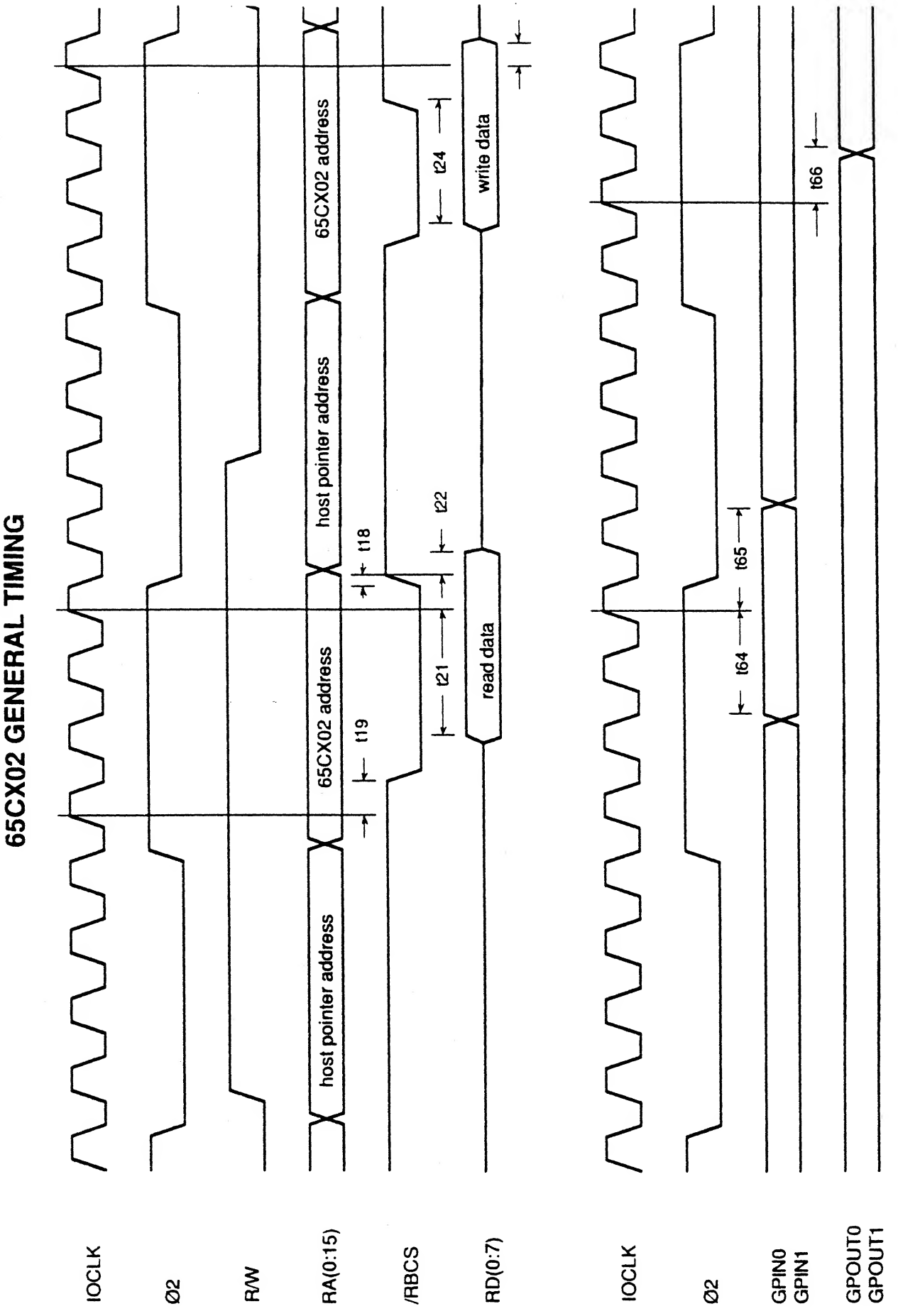

SERIAL TIMING
t1
t2
OCLK
CK3.6864 (INTERNAL)
GPIn
t54
t55
RTXCn
DPLL TIMING
t56
t57
DPCLK
DPLL STATE
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
t53
PCLK
t60 t59
RXDn
t58
RTXCn
t63
t67
RXDOn



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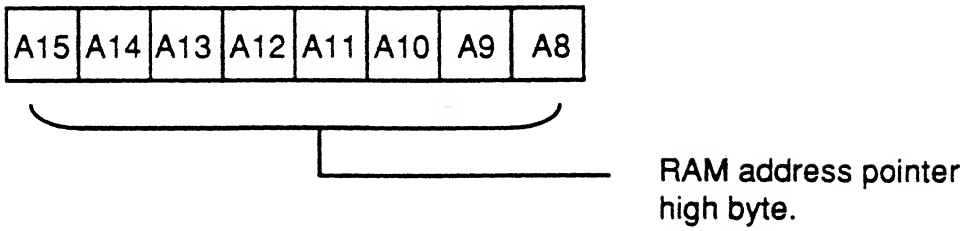
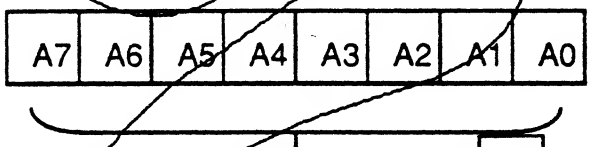
Address Offset $0
Read - RAM Address pointer high byte.
Write - RAM Address pointer high byte.



Bits A15:A8 - These bits form the high address of the 16 - bit host processor pointer to shared RAM. After each host processor access to RAM the Address pointer will increment by one.

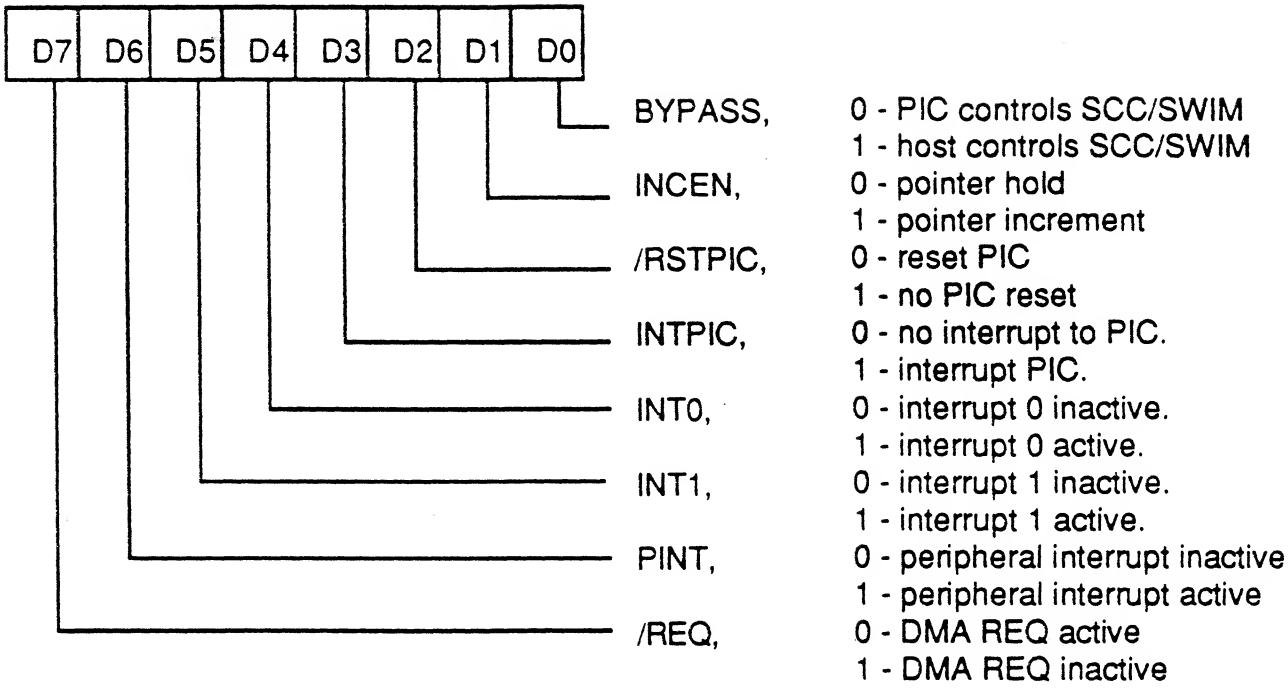
Address Offset $1
Read - RAM Address pointer low byte.
Write - RAM Address pointer low byte.



RAM address pointer
low byte.

Bits A7:A0 - These bits form the low address of the 16 - bit host processor pointer to shared RAM. After each host processor access to RAM the Address pointer will increment by one.

Address Offset $2
Read - Status/Control register.
Write - Status/Control register.



Bit D0 - is a read only bit which reflects the state of the PIC BYPASS signal. When this bit is set the host controls the peripheral port.

Bit D1 - INCEN is used to control the incrementing of the host address pointer. When this bit is set the host address pointer increments after each RAM access. Resetting this bit disables the auto-increment feature and causes the pointer to maintain a constant address during sequential RAM cycles.

Bit D2 - /RSTPIC is used to reset the peripheral interface controller. This bit is forced active by a system reset.

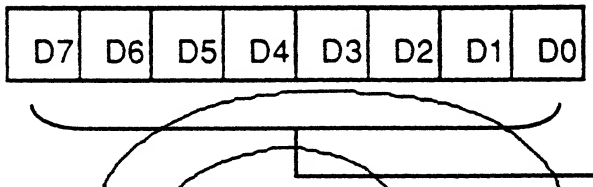
Bit D3 - INTPIC allows the host processor to interrupt the peripheral processor. This bit is asynchronously cleared by the peripheral processor.

Bits D5:D4 - The peripheral processor uses these bits to create host interrupt requests with different priority levels. The host processor can asynchronously clear these interrupts by storing a "1" to the respective bit. Storing a zero will leave the bit state unchanged.

Bit D6 - PINT is the peripheral port interrupt signal. It is used in the bypass mode only. In the non-bypass mode this signal is inactive.

Bit D7 - /REQ is low if either of the DMA request signals is active. It is used in the bypass mode only. When the PIC is in the non-bypass mode the /REQ signal is in its inactive state.

Address Offset $4
Read - Ram Data.
Write - Ram Data.

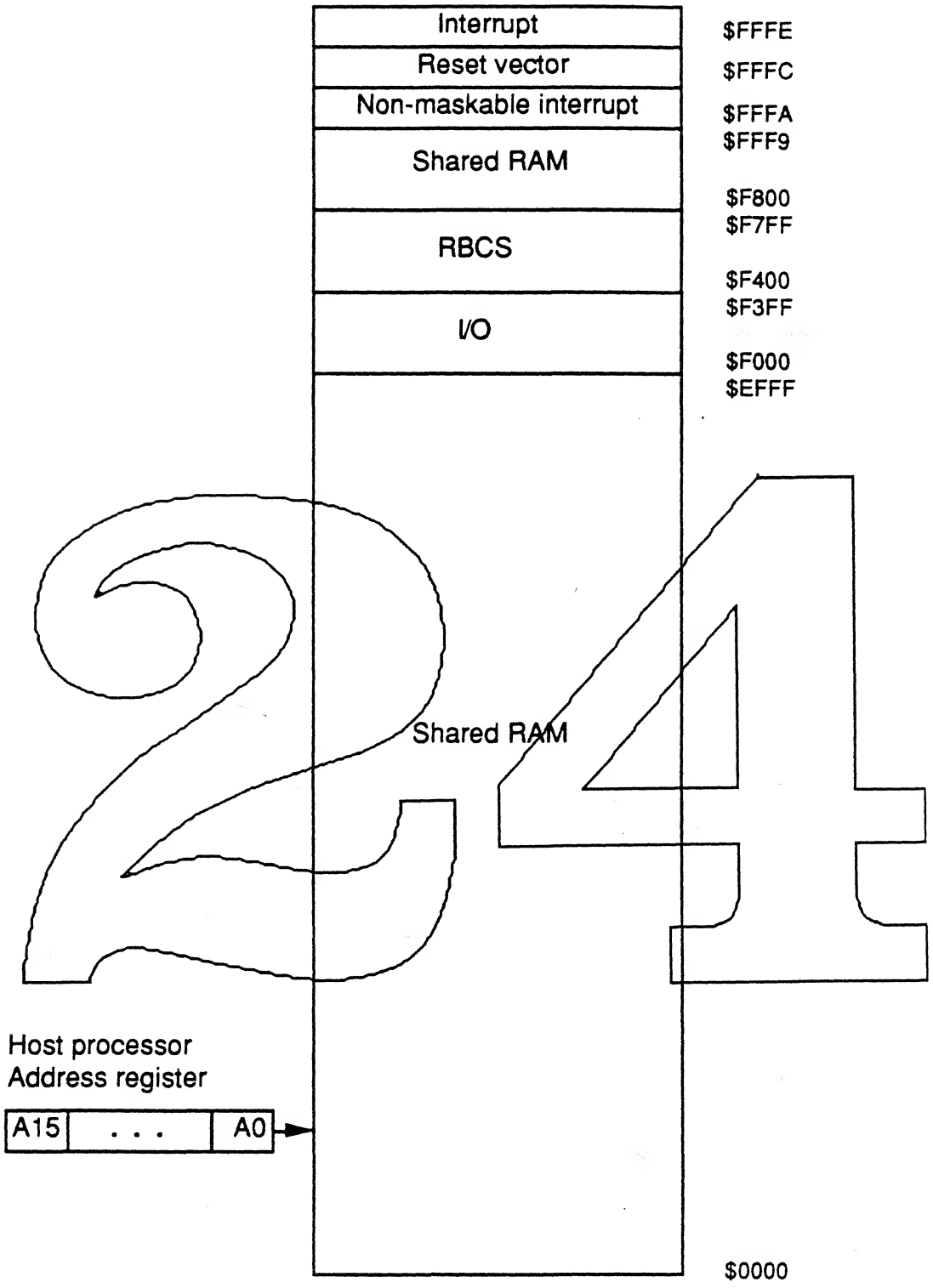


Shared Ram data.

Bits D7:D0 - These bits contain the shared ram data pointed to by the 16-bit address pointer register.

Address locations $10-1F are allocated to device registers. These registers are accessible by the host processor only in the bypass mode of operation.

	Device	
Address	SCC	SWIM
10	SCC B Command	Write Data
11	SCC A Command	Write Mark
12	SCC B Data	Write CRC
13	SCC A Data	Write Parameter RAM
14		Write Phase
15		Write Setup
16		Write Mode Zeroes
17		Write Mode Ones
18		Read Data
19		Read Mark
1A		Read Error
1B		Read Parameter RAM
1C		Read Phase
1D		Read Setup
1E		Read Status
1F		Read Handshake


Interrupt
Reset vector
Non-maskable interrupt
Shared RAM
RBCS
I/O
$FFFE
$FFFC
$FFFA
$FFF9
$F800
$F7FF
$F400
$F3FF
$F000
$EFFF
$0000
Shared RAM
Host processor
Address register
A15
. . .
A0

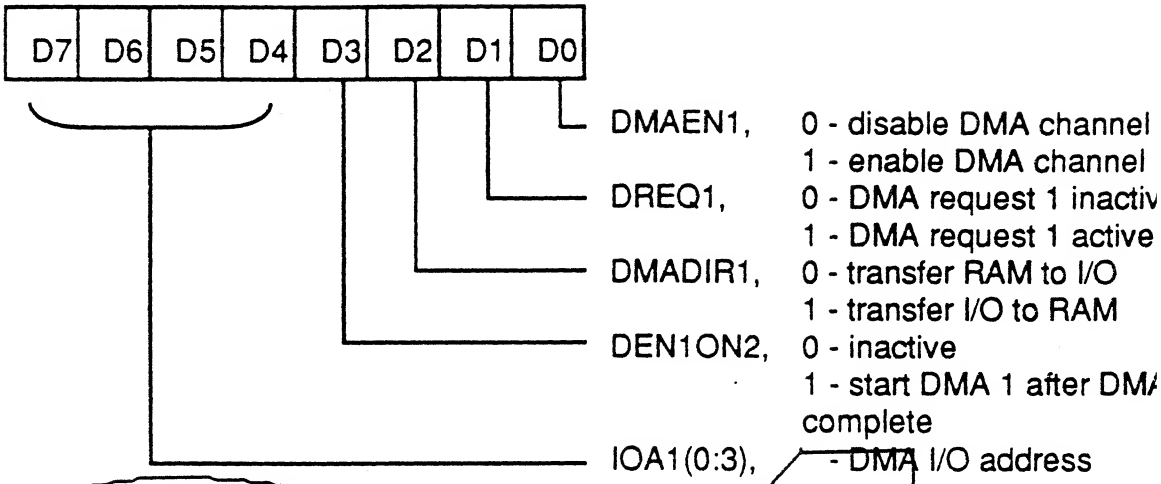
Address Offset $10
Read - Timer low counter, reset timer interrupt.
Write - Timer low latch.

Address Offset $11
Read - Timer high counter.
Write - Timer High latch, load counters, reset timer interrupt.

Address Offset $12
Read - Timer low latch.
Write - Timer low latch.

Address Offset $13
Read - Timer high latch.
Write - Timer high latch.

Address Offset $20
Read - DMA channel 1 control.
Write - DMA channel 1 control.



Bit D0 - DMAEN1 enables DMA channel 1 for transfers.

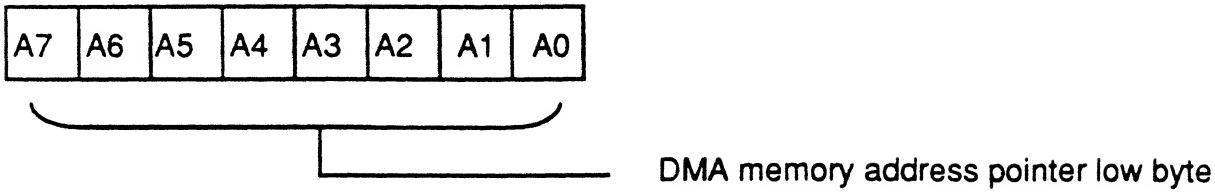
Bit D1 - DREQ1 reflects the state of the DMA request line for channel 1.

Bit D2 - DMADIR controls the direction of the DMA transfer. When DMADIR is low data is read from RAM and written to the SCC/SWIM. When DMADIR is high data is read from the SCC/SWIM and written to RAM.

Bit D3 - DEN1ON2 when set will automatically enable DMA channel 1 at the completion of a transfer over DMA channel 2.

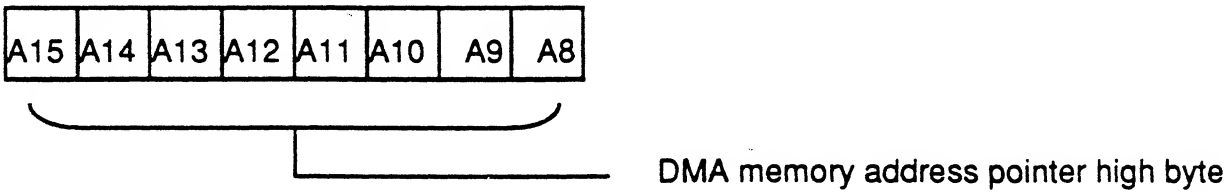
Bits D7:D4 - These bits define the SCC/SWIM address used during the DMA cycle.

Address Offset $21
Read - DMA channel 1 RAM address pointer low byte.
Write - DMA channel 1 RAM address pointer low byte.



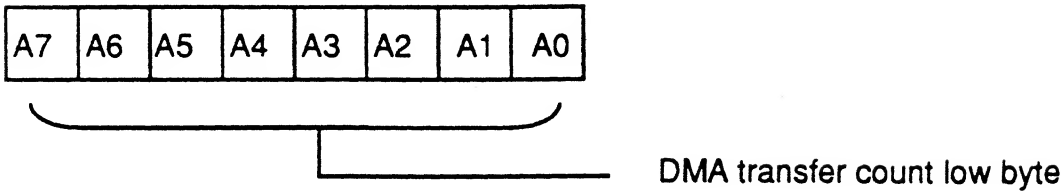
Bits A7:A0 - These bits form the low address of the 16 - bit DMA pointer to RAM. After each DMA access to RAM the Address pointer will increment by one.

Address Offset $22
Read - DMA channel 1 RAM address pointer high byte.
Write - DMA channel 1 RAM address pointer high byte.



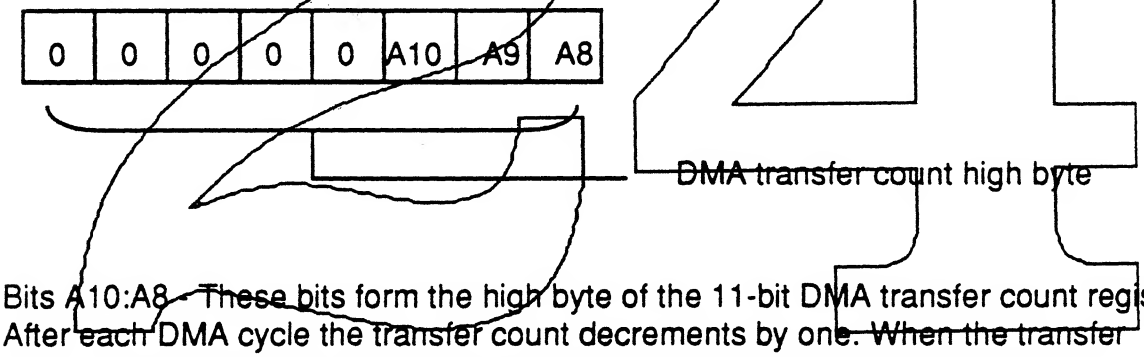
Bits A15:A8 - These bits form the high address of the 16 - bit DMA pointer to RAM. After each DMA access to RAM the Address pointer will increment by one.

Address Offset $23
Read - DMA channel 1 transfer count low byte.
Write - DMA channel 1 transfer count low byte.



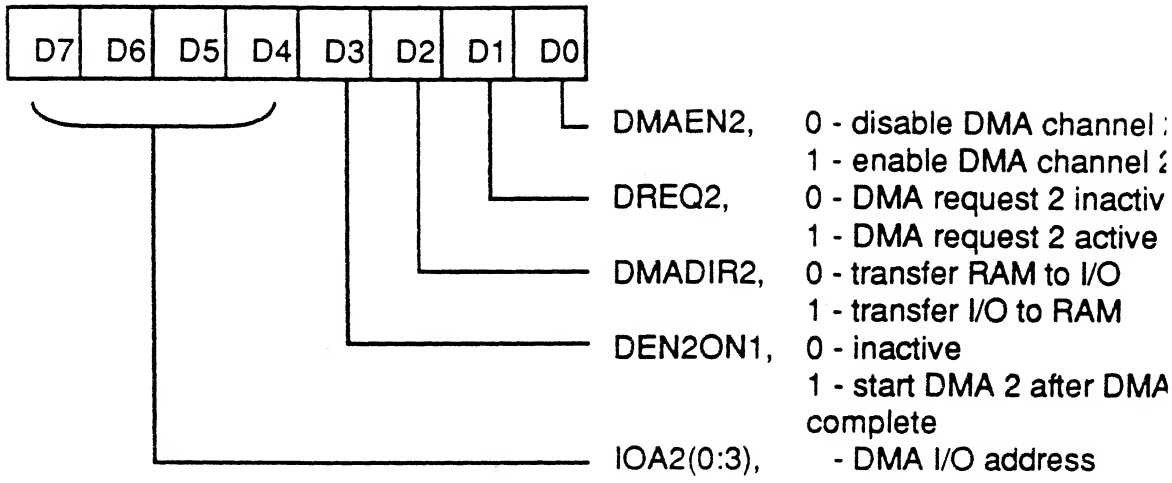
Bits A7:A0 - These bits form the low byte of the 11-bit DMA transfer count register. After each DMA cycle the transfer count decrements by one. When the transfer count reaches zero the DMA interrupt bit is set and further DMA requests are disabled.

Address Offset $24
Read - DMA channel 1 transfer count high byte.
Write - DMA channel 1 transfer count high byte.



Bits A10:A8 - These bits form the high byte of the 11-bit DMA transfer count register. After each DMA cycle the transfer count decrements by one. When the transfer count reaches zero the DMA interrupt bit is set and further DMA requests are disabled.

Address Offset $28
Read - DMA channel 2 control.
Write - DMA channel 2 control.



Bit D0 - DMAEN2 enables DMA channel 2 for transfers.

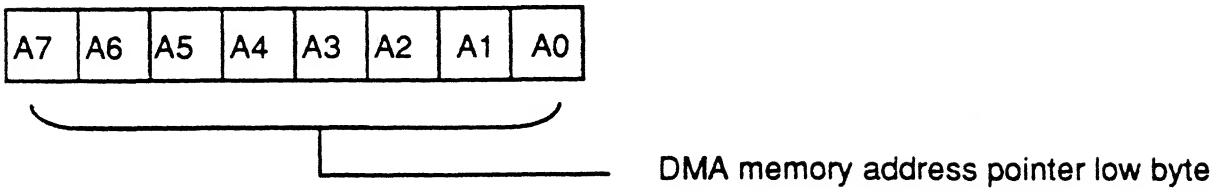
Bit D1 - DREQ2 reflects the state of the DMA request line for channel 2.

Bit D2 - DMADIR controls the direction of the DMA transfer. When DMADIR is low data is read from RAM and written to the SCC/SWIM. When DMADIR is high data is read from the SCC/SWIM and written to RAM.

Bit D3 - DEN2ON1 when set will automatically enable DMA channel 2 at the completion of a transfer over DMA channel 1.

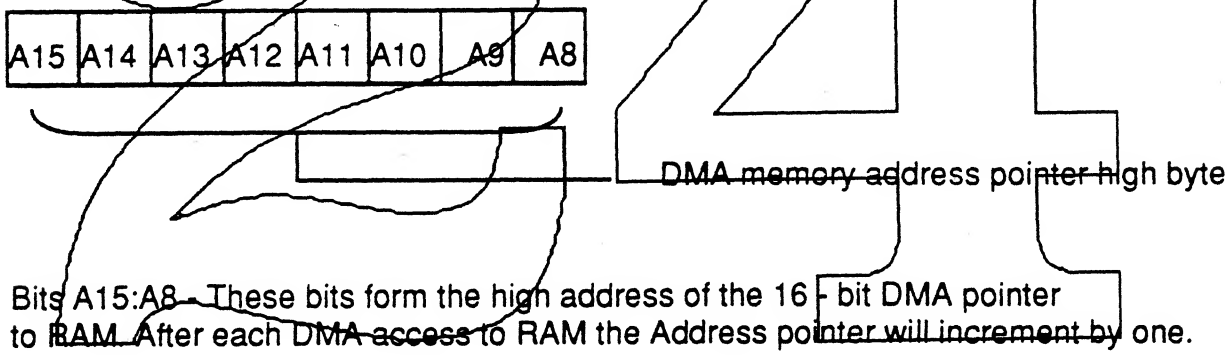
Bits D7:D4 - These bits define the SCC/SWIM address used during the DMA cycle.

Address Offset $29
Read - DMA channel 2 RAM address pointer low byte.
Write - DMA channel 2 RAM address pointer low byte.



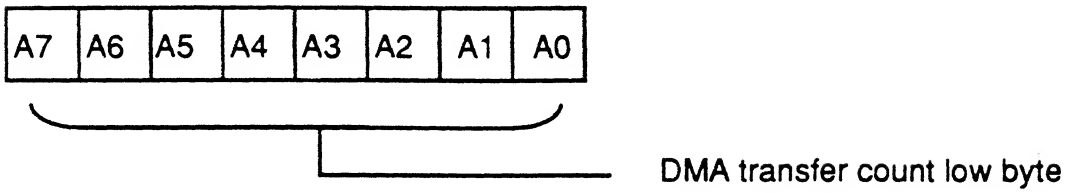
Bits A7:A0 - These bits form the low address of the 16 - bit DMA pointer to RAM. After each DMA access to RAM the Address pointer will increment by one.

Address Offset $2A
Read - DMA channel 2 RAM address pointer high byte.
Write - DMA channel 2 RAM address pointer high byte.



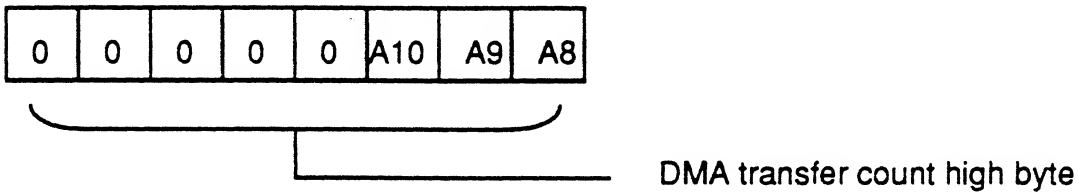
Bits A15:A8 - These bits form the high address of the 16 - bit DMA pointer to RAM. After each DMA access to RAM the Address pointer will increment by one.

Address Offset $2B
Read - DMA channel 2 transfer count low byte.
Write - DMA channel 2 transfer count low byte.



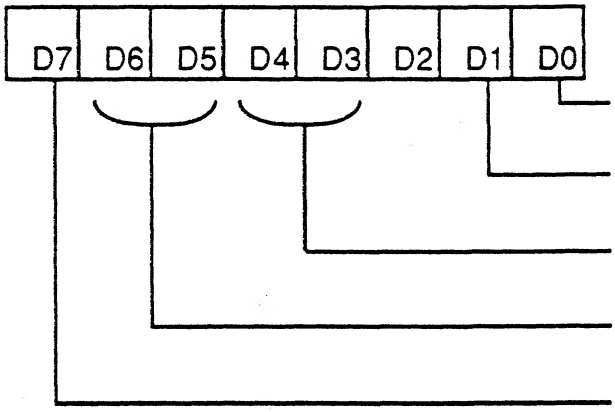
Bits A7:A0 - These bits form the low byte of the 11-bit DMA transfer count register. After each DMA cycle the transfer count decrements by one. When the transfer count reaches zero the DMA interrupt bit is set and further DMA requests are disabled.

Address Offset $2C
Read - DMA channel 2 transfer count high byte.
Write - DMA channel 2 transfer count high byte.



Bits A10:A8 - These bits form the high byte of the 11-bit DMA transfer count register. After each DMA cycle the transfer count decrements by one. When the transfer count reaches zero the DMA interrupt bit is set and further DMA requests are disabled.

Address Offset $30
Read - SCC control register.
Write - SCC control register.



BYPASS, 0 - 6502 controls SCC/SWIM
1 - Host controls SCC/SWIM

SCC*/SWIM, 0 - SCC port
1 - SWIM port

RTXCA(0:1), - encoded value which selects the SCC channel A clock sourc

RTXCB(0:1), - encoded value which selects the SCC channel B clock sourc

GPOUT1 0 - General purpose output 1 lov
1 - General purpose output 1 hig

Bit D0 - BYPASS determines which processor (Host or peripheral) controls the SCC/SWIM. This bit is set after a system reset.

Bit D1 - SCC*/SWIM selects the device which the PIC interfaces with. If SCC*/SWIM is low then the port is configured for use with the SCC. If SCC*/SWIM is high then the port is configured for the SWIM. In the SWIM mode the polarity of the DMA request signals are changed to active high.

Bits D4:D3 - these bits represent an encoded value used to multiplex one of four clock sources onto the RTXCA signal. A table listing the clock sources is given below.

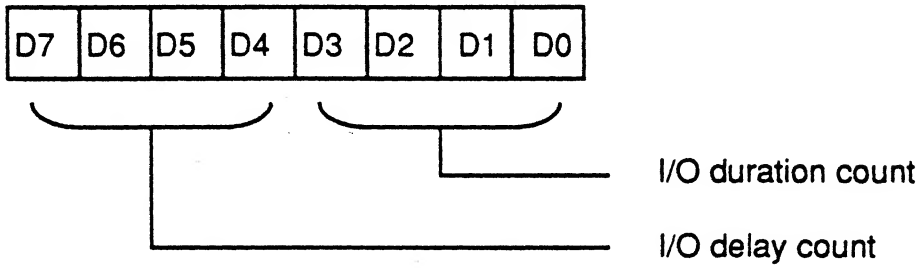
D4:D3	RTXCA source
00	3.6864MHz
01	DPCLK/10
10	Digital phase locked loop output
11	GPIA

Bits D6:D5 - these bits represent an encoded value used to multiplex one of four clock sources onto the RTXCB signal. A table listing the clock sources is given below.

D6:D5	RTXCB source
00	3.6864MHz
01	DPCLK/10
10	Digital phase locked loop output
11	GPIB

Bit D7 - GPOUT1 controls the state of general purpose output 1.

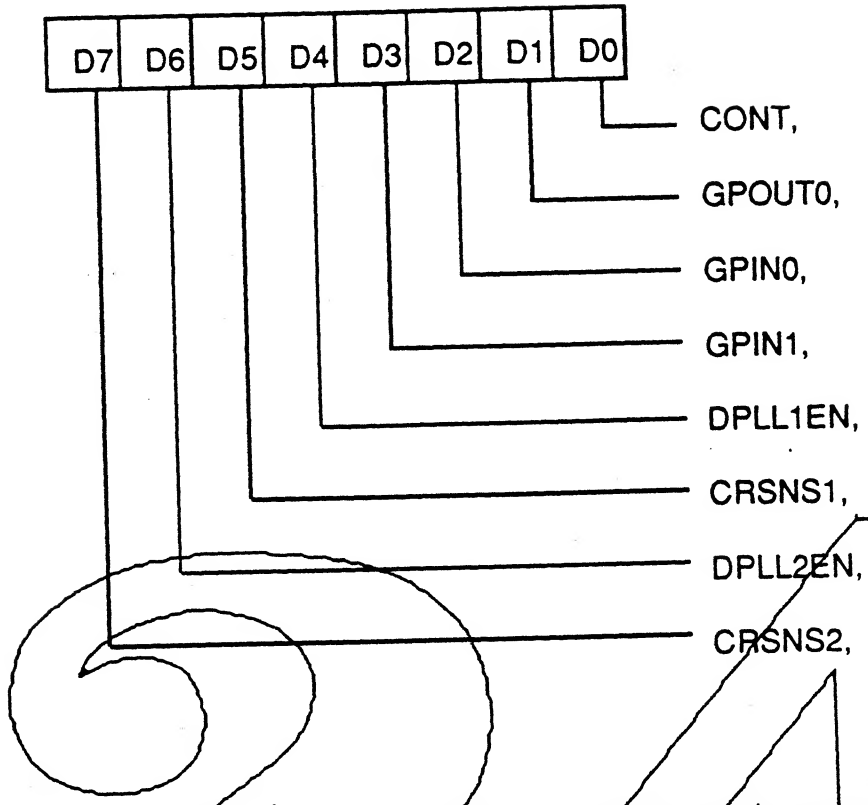
Address Offset $31
Read - I/O Control register
Write - I/O Control register.



Bits D3:D0 - These bits are used to program the duration of the SCC/SWIM chip-select. The chip-select duration is equal to the count+1 multiplied by the IOCLK period. These bits are set after a system reset.

Bits D7:D4 - These bits are used to program the holdoff interval between sequential SCC/SWIM accesses. The holdoff delay is equal to the count multiplied by twice the IOCLK period. These bits are set after a system reset.

Address Offset $32
Read - Timer/DPLL control.
Write - Timer/DPLL control.



Bit D0 - This bit selects between the one-shot mode and continuous mode of timer operation. In the one-shot mode the timer interrupt bit is set when the cou reaches zero. After counting to zero the timer underruns and continues to count further interrupts are disabled. In the continuous mode the timer generates interru spaced at constant time intervals.

Bit D1 - GPOUT0 controls general purpose output 0.

Bit D2 - GPIN0 reflects the state of general purpose input 0.

Bit D3 - GPIN1 reflects the state of general purpose input 1.

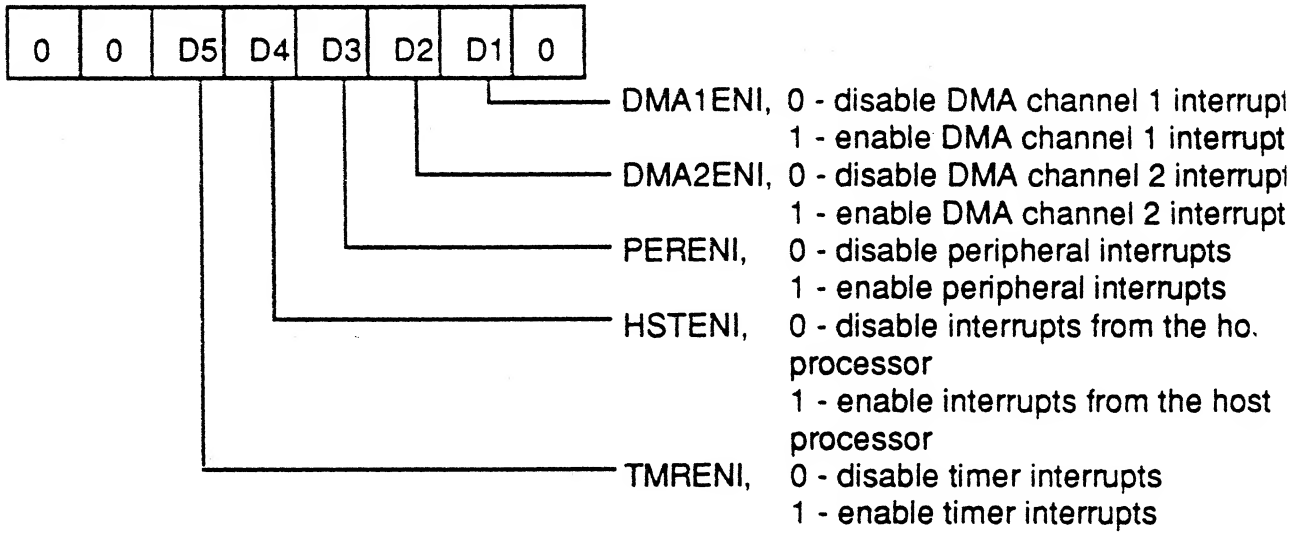
Bit D4 - DPLL1EN forces the DPLL for channel A to begin searching for clock information on the RXDA signal source. Clock information is recovered at a freq of DPCLK/10 and output on the RTXCA signal line. The RTXCA clock signal is 9 degrees out of phase with the RXDA transition information in order to permit the PIC to recover FM0 data from the receive signal. The recovered data is placed on the RXDAO output in NRZ format.

Bit D5 - CRSNS1 is valid whenever clock activity is detected on the RXDA signa CRSNS1 is reset if clock activity is absent for more than 128 DPCLK cycles.

Bit D6 - DPLL2EN forces the DPLL for channel B to begin searching for clock information on the RXDB signal source. Clock information is recovered at a freque of DPCLK/10 and output on the RTXCB signal line. The RTXCB clock signal is 90 degrees out of phase with the RXDB transition information in order to permit the SCC to recover FM0 data from the receive signal. The recovered data is placed on the RXDBO output in NRZ format.

Bit D7 - CRSNS2 is valid whenever clock activity is detected on the RXDB signal. CRSNS2 is reset if clock activity is absent for more than 128 DPCLK cycles.

Address Offset $33
Read - Interrupt mask register.
Write - Interrupt mask register.



Bit D1 - DMA1ENI disables interrupts from DMA channel 1.

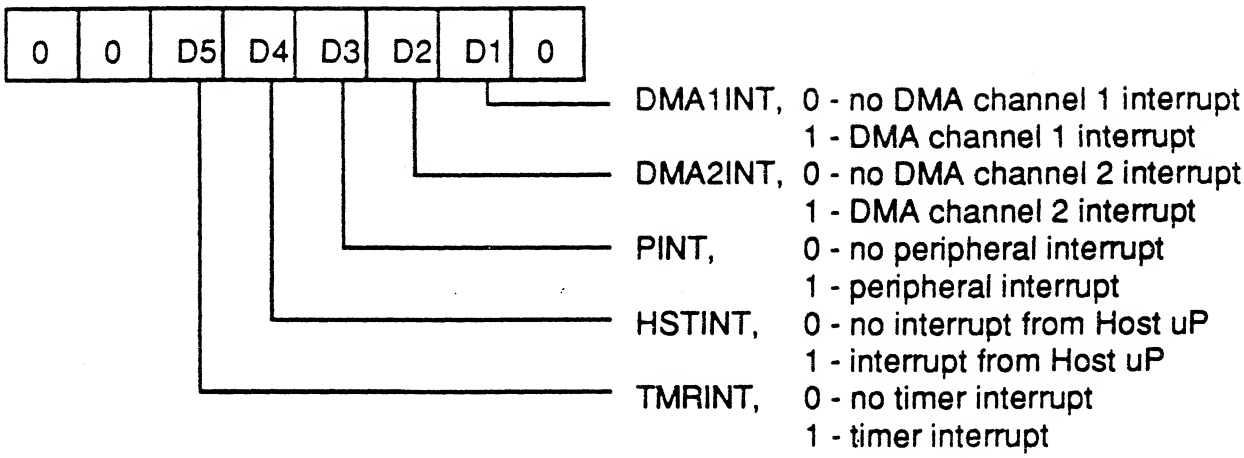
Bit D2 - DMA2ENI disables interrupts from DMA channel 2.

Bit D3 - PERENI allows the peripheral processor to disable interrupts from the peripheral port.

Bit D4 - HSTENI allows the peripheral processor to disable interrupts from the host processor.

Bit D5 - TMRENI disables interrupts from 16-bit timer.

Address Offset $34
Read - Interrupt register.
Write - Interrupt register.



Bit D1 - DMA1INT is set at the end of a DMA transfer. This bit can be reset by storing a "1" to it. Storing a zero will leave the bit state unchanged.

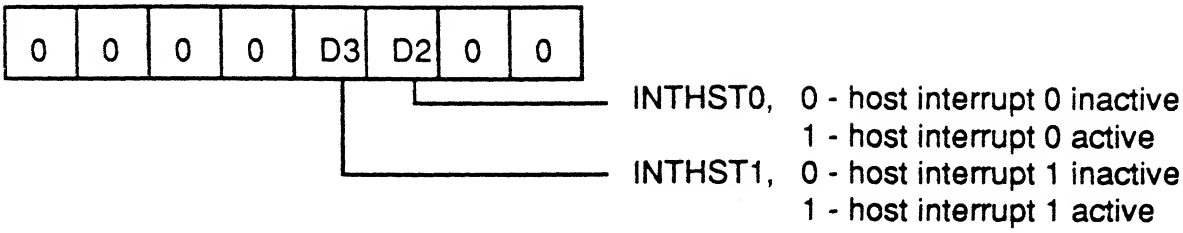
Bit D2 - DMA2INT is set at the end of a DMA transfer. This bit can be reset by storing a "1" to it. Storing a zero will leave the bit state unchanged.

Bit D3 - PINT monitors the state of the peripheral interrupt request line. In the BYPASS mode of operation this bit is disabled and in its inactive state.

Bit D4 - HSTINT indicates that the host processor has requested interrupt service. This bit can be reset by storing a "1" to it. Storing a zero will leave the bit state unchanged.

Bit D5 - TMRINT reflects the state of the timer interrupt request output. This bit can be reset by storing a "1" to it or by reading the timer low order counter. Storing a zero will leave the bit state unchanged.

Address Offset $35
Read - Host register.
Write - Host register.



Bits D3:D2 - Storing a "1" to either of these bits will generate a host processor interrupt. These bits are asynchronously cleared by the host processor.

Peripheral Processor I/O map

Base address $F000

Address locations $40-4F are allocated to device registers. These registers are accessible by the peripheral processor only in the non-bypass mode of operation.

Address	Device: SCC	Device: SWIM
40	SCC B Command	Write Data
41	SCC A Command	Write Mark
42	SCC B Data	Write CRC
43	SCC A Data	Write Parameter RAM
44		Write Phase
45		Write Setup
46		Write Mode Zeroes
47		Write Mode Ones
48		Read Data
49		Read Mark
4A		Read Error
4B		Read Parameter RAM
4C		Read Phase
4D		Read Setup
4E		Read Status
4F		Read Handshake